On Modeling of Linear-Assisted DC-DC Voltage Regulators

Nasima Sedaghati, Herminio Martínez-García, and Jordi Cosp-Vilella
Department of Electronics Engineering
Eastern Barcelona School of Engineering (EEBE). Diagonal-Besòs Campus.
Technical University of Catalonia (UPC). BarcelonaTech
Eduard Maristany Ave., nº 10 – 14.
E-08019 – Barcelona, SPAIN
nasima.sedaghati@estudiant.upc.edu ; { herminio.martinez; jordi.cosp }@upc.edu

***Abstract*—This paper presents the modeling of linear-assisted DC-DC regulators. This kind of voltage regulators consists of a switching converter together with a classic or LDO (low drop-out) linear voltage regulator. While the linear regulator provides the constant output voltage, the switching converter conducts nearly all the current provided in the output load, and keeping the regulator current close to zero where the higher efficiency is achieved. However, the circuit could be unstable due to some critical parameters such as parasitic output capacitance; as a consequence, the mathematical modeling is obtained to study and corroborate the stability of the whole system.**

***Keywords*—DC-DC converters; LDO regulator; MATLAB/SIMULINK; power electronics**

I. INTRODUCTION

DC-DC switching power converters have been used as a modern power supply in the past decades [1, 2]. DC-DC switching converters could provide ripple in the output voltage due to the switching process; thus, the use of linear regulator would be necessary to eliminate this ripple and produce the surplus of the current that is not provided by the switching converters. Linear regulators used in power converters could be either classic linear or LDO regulator. In this paper, a LDO regulator is used that has advantages of maximizing the usage of available input voltage and it can work with smaller drop-out voltage. Therefore, as a consequence, it has less internal power loss, which are one of the critical points (among other) in linear regulators, resulting in voltage regulators with higher efficiency [3].

Previous researches have been done to minimize the existing impediments such as low efficiency and high power dissipation [4, 5]. In this article, a proposal of linear-assisted DC-DC converter and its modeling is presented to inquire the control loop stability. In fact, in order to carry out the stability study, a model of the whole system is necessary.

II. STRUCTURE OF LINEAR-ASSISTED CONVERTER

In the proposed circuit shown in Fig. 1, the switching converter is connected in parallel with a LDO regulator, providing the desired output current and voltage by the load. As it is well known, the LDO regulator with the feedback loop of R_1 and R_2 continuously compares the reference and the output voltages in the input ports in order to provide a constant output voltage. This output voltage is given by:

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{ref1} \tag{1}$$

Since the output current is obtained by the sum of regulator and the switching current, and is a constant value, the conduction and cut of the switch is controlled by the comparator (*CMP*) to conduct the majority of the output current by the switching converter. Consequently, the analog comparator compares a reference voltage, V_{ref2}, with the regulator's sensed current flowing through the linear regulator. This reference voltage, V_{ref2}, fixes a boundary current or threshold current, to control the switching frequency [6]. The current sensing through the linear regulator is done by a resistor of 1 ohm and is defined by the following expression:

$$I_\gamma = \frac{V_{ref2}}{R_{sense}} \tag{2}$$

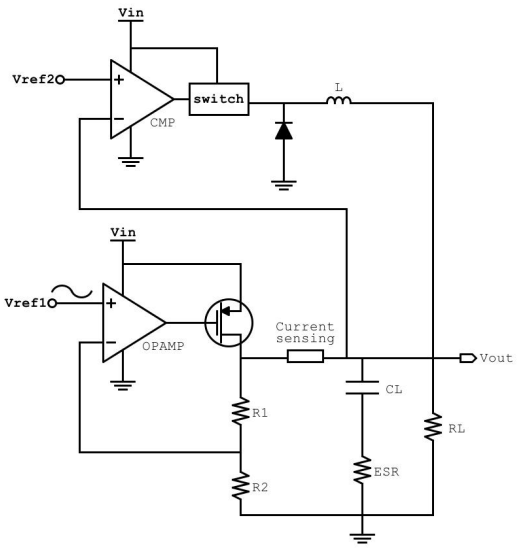

Fig. 1. Proposed schematic of the linear-assisted dc-dc converter

978-1-5090-4565-5/16/$31.00 ©2016 IEEE

The operation of the circuit is as follow: On the one hand, when the load current is below the threshold current, the output of comparator will be low and will set the switch off. Thus, the current through the inductor L will decrease, and the regulator current will increase to provide all the output current that flows through the load. However, on the other hand, when the load current increases, the comparator will pass to high and turns on the switch of the switching converter. Therefore, the inductor current I_L will increase. This makes the regulator current to decrease linearly as it can be seen in Fig. 2. All the simulations are based on a 0.35-µm CMOS technology in Virtuoso Cadence.

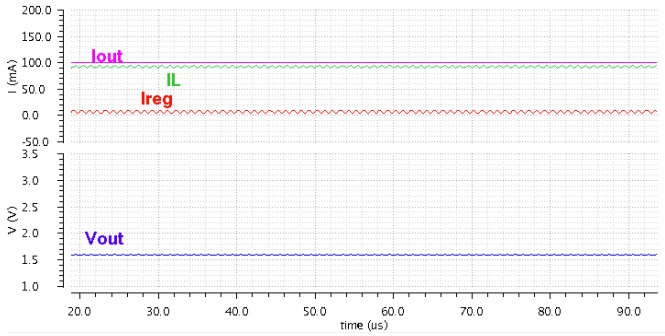

Fig. 2. Transient response of dc/dc converter

In this simulation, it can be observed that with the input voltage of 3.3 V, a constant value of 1.65 V is obtained at the output terminals, and the load current is fixed at 100 mA that is mostly provided by inductor current. Therefore, it keeps the regulator current close to zero. In Fig. 3, the transient response of the circuit with the variation of V_{in} from 3.3 V to 4.3 V is shown, and it demonstrates a good line regulation as well as the load regulation from 200 mA to 300 mA variation of load current I_{out}.

III. MODELING OF THE PROPOSED CIRCUIT

It is necessary to study the mathematical modeling of the proposed circuit to consider the critical parameters and analyze the circuit's behavior by the variation of those values to observe the stability of the whole system. In Fig. 4 a simplified modeling block diagram of linear-assisted converter is shown. In this model, the linear regulator current (I_{LIN}) is obtained from the output current, I_{out}, and the switching converter current, I_{sc}:

$$I_{LIN} = I_{out} - I_{sc} \tag{3}$$

On the one hand, Fig. 5 shows the DC-DC buck converter circuit. The buck converter is considered with an ideal switch that has the switching period of T. When the switch is ON, the current through the inductor (L), load capacitor (C_L) and its equivalent series resistor (ESR) is derived from the equations below:

$$i_{sc}(t) = i_L(t) - i_c(t) \tag{4}$$

$$i_L(t) = \frac{1}{L}\int (v_{in}(t) - v_{out}(t))\,dt \tag{5}$$

$$v_{out}(t) = v_c(t) + v_{ESR}(t) = \frac{1}{C}\int i_c(t)\,dt + ESR \cdot i_c(t) \tag{6}$$

$$i_c(t) = C\frac{dv_{out}(t)}{dt} - C \cdot ESR \cdot \frac{di_c(t)}{dt} \tag{7}$$

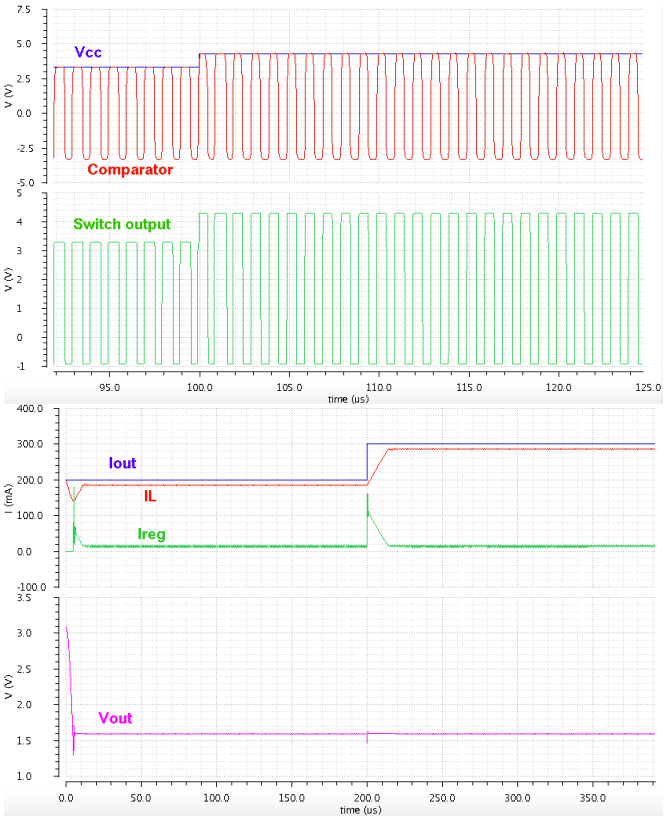

Fig. 3. Transient response for line and load regulation respectively

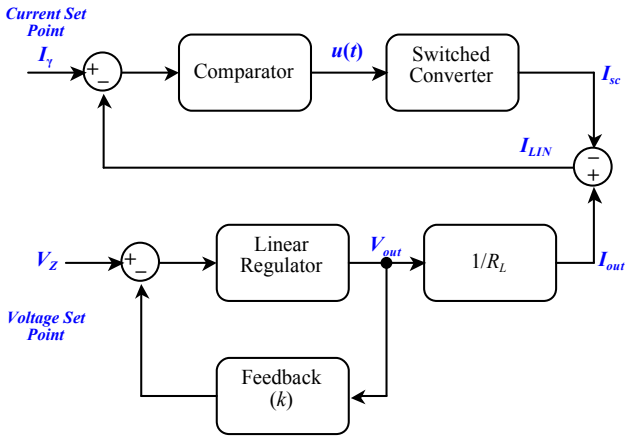

Fig. 4. Block diagram of the modeling of linear-assisted converter

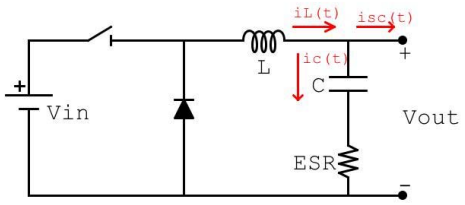

Fig. 5. Basic DC-DC buck converter circuit

The obtained expressions (5) and (7) are implemented in Matlab/Simulink® as indicated in Fig. 6 using linear blocks (summing, gains, etc. blocks) subsequently applied to integrator and derivative blocks to obtain the switching converter's output current (i_{sc}).

On the other hand, the linear regulator block consists of an error amplifier (Fig. 7), pass transistor and the feedback loop. To obtain the transfer function for each block, the equivalent circuits are shown below. The transfer function of the operational amplifier is given by equation (8) and it demonstrates two poles (P_1, P_2) and a zero (Z) made by miller capacitor (C_c).

$$H_{oa}(s)=\frac{V_m}{V_{ref}}=\frac{A_{oa}\left(1-\frac{s}{Z}\right)}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)} \tag{8}$$

$$\begin{cases} A_{oa}=g_{m1}g_{m2}\times r_{o1}r_{o2} \\ Z=g_{m2}/C_c \\ P_1=1/g_{m2}r_{o1}r_{o2}C_c \\ P_2=g_{m2}/C_2 \end{cases} \tag{9}$$

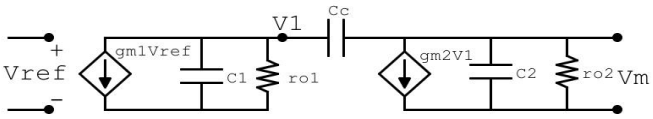

Fig. 7. operational amplifier's equivalent circuit with miller effect (C_c)

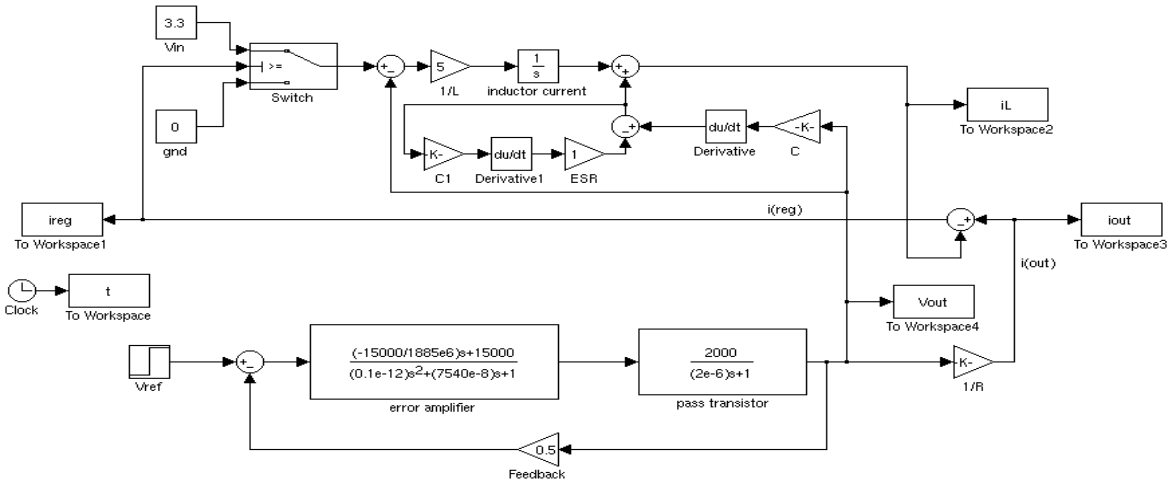

Fig. 6. Proposed linear-assisted converter modeling diagram

Fig. 8 shows the equivalent circuit of pass transistor and the transfer function of pass transistor is calculated in expression (10) and it depends on the gain of transistor ($g_m r_{pass}$) and its capacitor C_{pass}.

$$H_{pass}(s)=\frac{V_{out}}{V_m}=\frac{g_m\times r_{pass}}{1+C_{pass}r_{pass}s} \tag{10}$$

The feedback value that we introduced earlier in equation (1) obtained from the ratio $R_2/(R_1+R_2)$ and is applied to the inverter input of op.amp.

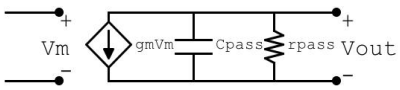

Fig. 8. Pass transistor equivalent circuit

IV. Simulations and Results

The proposed model that is introduced in the previous section, guaranties the constant output voltage by linear regulator. Fig. 9 indicates the simulation results in Matlab/Simulink® that matches with the results obtained in Virtuoso cadence.

The circuit could be unstable due to some parameters such as output capacitor and its equivalent series resistor. In fact, the existence of these parameters is important in order to predict the transient behavior of the converter. The frequency response of the circuit is also quite sensitive to output capacitor (C_L) and its ESR that is connected to the load resistor.

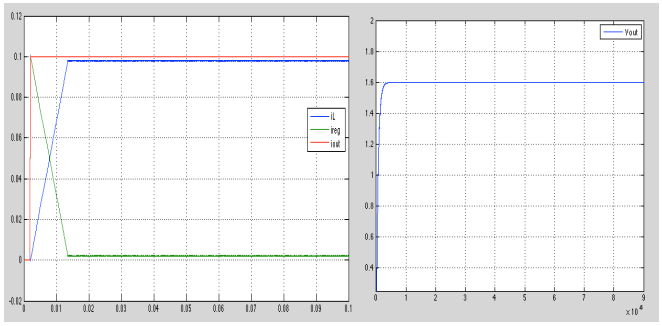

Fig. 9. Transient response of the proposed model in Matlab/Simulink®

In Fig. 10, experimental results for different values of C_L are obtained. The closed-loop gain is 6 *dB* since we have an output voltage, two times bigger than input voltage. For an output capacitor of 100 *nF*, the gain and phase margin are 59.8 *dB* and 50 degrees, respectively. In these conditions, the gain margin for C_L=100 *pF* is reduced to 20 *dB*, and phase margin increased to 114º. As it is obtained in fig. 11, for the C_L=10 µ*F* and ESR=0.1 Ω, a significant reduction in phase margin is observed and by changing the ESR to 1 Ω, gain margin of about 60 *dB*, and phase margin of 117º is calculated. It is also observed that varying the gain of operational amplifier does not affect the stability of the converter.

V. CONCLUSION

In this paper, the simulation of linear-assisted DC-DC converters based on 0.35 µm CMOS technology and its modeling in Matlab/Simulink® has been shown. LDO regulator in this structure used, that has a control loop with possible instability. Thus, the proposed modeling has helped to characterize the critical parameters such as output capacitance and its equivalent series resistance. From this modeling the system could be easily improved by varying the parameters value.

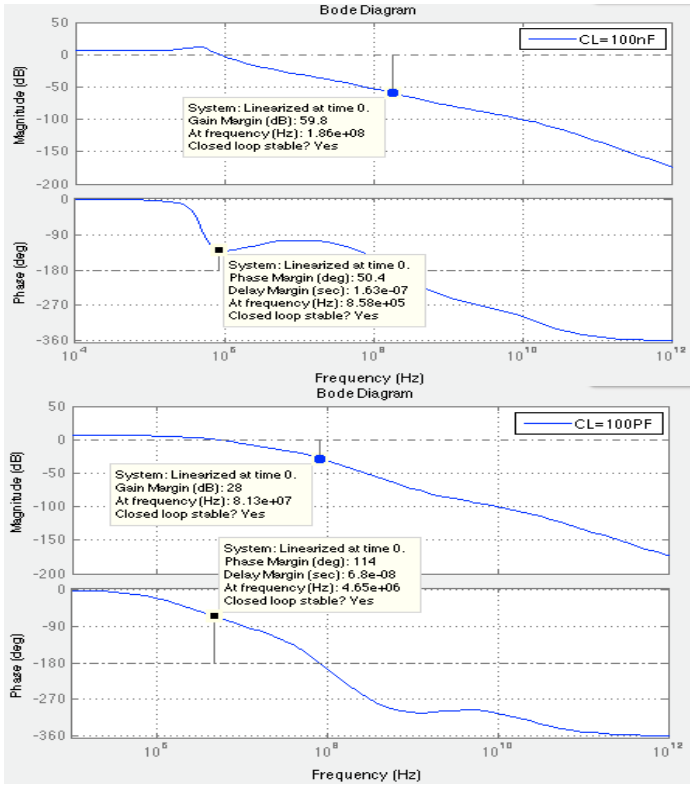

Fig. 10. Bode plot for C_L=100 *nF*, and 100 *pF*

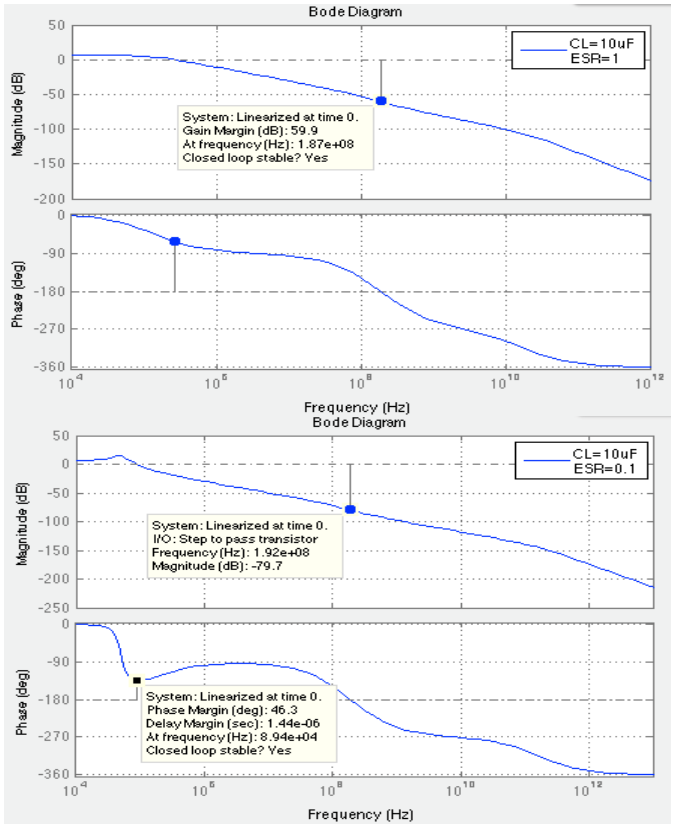

Fig. 11. Bode plot for C_L=10 µ*F*, and ESR=1 Ω and 0.1 Ω

ACKNOWLEDGMENT

This work has been partially supported by the Spanish Ministerio de Economía y Competitividad by Project DPI2013-47799-C2-2-R, and the European Union by Project CargoANTs – FP7-SST-2013-605598.

REFERENCES

[1] Erickson, R.W. and D. Maksimovic, "Fundamentals of power electronics," 2007: Springer Science & Business Media.

[2] Di Piazza, M.C. and G. Vitale, "DC/DC Power Converters, in Photovoltaic Sources," 2013, Springer. p. 203-251.

[3] Rincon-Mora, G.A. and P.E. Allen, "Optimized frequency-shaping circuit topologies for LDOs," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, 1998. 45(6): p. 703-708.

[4] Martinez, H. and A. Conesa. "Modeling of linear-assisted DC-DC converters," in Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on. 2007. IEEE.

[5] Ertl, H., J.W. Kolar, and F.C. Zach, "Basic considerations and topologies of switched-mode assisted linear power amplifiers," Industrial Electronics, IEEE Transactions on, 1997. 44(1): p. 116-123.

[6] Martinez, H. and A. Conesa. "Linear-assisted DC-DC converter based on CMOS technology," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE. 2008. IEEE.